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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,758	03/07/2002	Tien M. Nguyen	D-422	2860

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EXAMINER	
WONG, LINDA	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/092,758	NGUYEN ET AL.	
	Examiner	Art Unit	
	LINDA WONG	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/4/2008 has been entered.

Response to Arguments

2. Applicant's arguments filed 2/4/2008 have been fully considered but they are not persuasive.

3. The applicant contends

> "Marko uses a recovered data signal as the input that is not the baseband waveform signal encoding a data bit stream, (and this gives rise to Marko having the MAJOR error while the present invention does not)"

The examiner respectfully disagrees. The limitation recites "a pulse detector for generating data transition pulses from the baseband signal waveform". The applicant contends the present invention does not "represent the baseband waveform signal by a digital bit stream". The examiner would like to point out that the recited limitations does not indicate how or what component is being used within the pulse detector for generating transition pulses from the baseband signal waveform. Furthermore, the limitation recites "data transition pulses" are generated from "the baseband waveform." Marko discloses "recovering timing of the narrow bandwidth recovered clock with respect to receive baseband data timing." This

indicates that the baseband timing is being used within the phase detector as shown in Fig. 9b. The timings are determined by the transition detector also shown in Fig. 9b. Since the transition detector is a sampler, the input must be a baseband waveform or baseband signal since the output are baseband data timings. (Col. 8, lines 63-67) Thus, based on the recited limitation, Marko discloses the pulse detector or transition detector generates "data transition pulses from the baseband signal waveform".

4. The applicant further contends

> "because Marko's early and late increments are based upon phase detection of transitions of the recovered data signal and the recovered clock and not based on pulses generated from the baseband waveform signal, (as there is a clear difference between the generation of early and late events, where Marko compares transitions of the recovered data and recovered clock signals, whereas, the present invention uses a search window between the transition pulses and the adjusted timing pulses)"

As discussed above, Marko discloses "generating data transition pulses from the baseband signal waveform". Furthermore, Marko discloses "the phase detector 426 then generates early/late signals 430 based on the phase of the incoming signal 406. The early/late transition signal 430 is forwarded to a wide bandwidth filter (accumulator) 432 which accumulates the number of early/late transitions and compares the number to a predetermined threshold." Since the input signal to the phase detector are data transition pulses from the baseband signal waveform as discussed above, the phase comparison determined by the phase detector would be based on the clock, Fig. 9b, label 980 or Fig. 9a, label 938, and the transitions of the baseband signal as shown in Fig. 9a and 9b.

5. The applicant also contends

> "because the phase error in Marko is determined from transitions of two digital signals, and not from transition pulses (where Marko adjusts the recovery clock having the MINOR errors that is coupled to the MAJOR timing bit boundary errors by phase detection comparison to the recovery data, whereas the present invention adjusts the adjusted timing pulses having the MINOR reference clock errors but without coupling the MINOR errors to any MAJOR errors)".

The applicant indicates the present invention "adjusts the timing pulses having minor reference clock errors but without coupling the minor errors to any major errors." The examiner would like to point out the recited limitation does not recite adjusting the timing pulse requires adjusting the pulses having minor or major errors. The limitation recites "a timing pulse delay adjustor for adjusting an adjusted timing pulse delay communicated to the pulse detector for delaying the adjusted timing pulses for synchronizing the adjusted timing pulses with the data transition pulses and with the baseband signal over a plurality of bit periods when the running count exceeds the predetermined threshold count value." Marko discloses the recovered clock is adjusted based on the comparison as shown in Fig. 9b, label 966, wherein a phase adjustment is made. (Col. 4, lines 18-39) When adjusting the phase, the time or delay of the timing is adjusted as well.

6. The applicant contends

> "Marko does not anticipate the present invention because 1) Marko uses a recovered data signal as the input and not the baseband waveform encoding a data bit stream; 2) because Marko's early and late increments are based upon transitions of the recovered data signal and not based on precise transition pulses generated from the baseband waveform; and 3) because the phase error in Marko is determined from transitions of a digital bit stream, and not from transition pulses of zero crossings from baseband waveform, resulting in phase error that is a coupling of the bit boundary timing errors with reference clock timing errors".

The examiner respectfully disagrees. Regarding remark 1), please refer to the rebuttal above. Regarding remark 2), based on the rebuttal of 1), Marko's invention

calculates the increments of the early and late signals based on the transitions of the baseband signal, wherein the baseband signal is generated from the transition detector. As previously stated, the input to the transition detector would be a baseband waveform or baseband signal, since the output of the transition detector are baseband data timings. Regarding remark 3), as discussed, Marko discloses baseband data timings are inputted into the phase detector. The claim only recites limitations regarding the pulse or phase detector generating data transition pulses and comparing the data with adjusted timing pulses to generate early and late signals for the purpose of synchronization. The claim does not recite limitations regarding the zero crossings of the baseband signal.

7. The applicant further contends

"Marko does not suggest the present invention, at least, because: i) Marko teaches away from the present invention by firstly demodulating the received signals into a recovered data signals in advance of data detection introducing bit boundary timing errors, which is completely contrary to applicant's data detection directly upon zero crossings of the baseband waveform, 2) because Marko's demodulation of the received signals into the recovered data signals injects jitter errors due to discrete 1/32 bit boundaries quantization, that is counter-intuitive to the use of zero crossings of baseband waveform signals. Applicant requests allowance of claims".

The examiner respectfully disagrees. Regarding remark 1), although Marko demodulates the received signals into a recovered signal so to produce baseband data timing signals as shown in Fig. 9b and discussed in Col. 8, lines 63-67, the claim does not recite limitations regarding how the data transition pulses are generated from the baseband signal waveform. Thus, based on the broadest interpretation of the claimed language, Marko discloses the limitation. Please refer to the rebuttal above for further information. Regarding remark 2), please refer to the rebuttals above regarding Marko demodulating the received signal. Although

Marko differs from the present invention in the use of zero crossings of baseband waveform signals, the claimed limitations fails to recite information regarding the present inventions use of zero crossing.

Note: The examiner would like to remind the applicant that the prior art rejection is geared towards the recited limitations and the examiner reviews the claims based on the broadest interpretation. Furthermore, examination is performed in light of the specification, **without** reading the specification into the claim. It seems to the examiner that the remarks provided on 2/4/2008 is geared towards specific operational differences between the prior art and present invention but the claimed language does not reflect those differences. The examiner would also like to emphasize the pertinent prior art references cited below. Such references also read on the limitations of the claim. **Please review the recited references.** Due to the rebuttal above, the rejection stands as previously stated.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. **Claims 1-3,5-7,9** are rejected under 35 U.S.C. 102(b) as being anticipated by Marko et al (US Patent No.: 5463351).

   a. **Claim 1**,

i. Marko et al discloses:

- A data transition generator (Fig. 9b, label 948) for generating data transition pulses from a received baseband signal (Col. 7, lines 30-33, Col. 1, lines 55-62), wherein the received signal is inherently a self clocked signal. The received signals are further transmitted/received by a receiver front end coupled to a time division multiplexer for providing time division multiplexed framed digital signals. Framed digital signals would inherently comprise multiple or many bits within a frame or period. (Col. 2, lines 51-67 and Col. 3, lines 1-5) Since the data transition pulses are generated from the received signals, wherein the received signals contain bits within a frame, the data transition pulses are in synchronous with the received signal.
- A phase detector (Fig. 9b, label 950) for comparing the data transition pulses (Fig. 9b, label 948) with the adjusted timing pulses (Fig. 9b, label wide BW recovered clock) for generating early and late signals (Fig. 9b, labels early/late), wherein the early and late signals are inherently generated when the data transition pulses (Fig. 9b, output from label 948) leads or lags the adjusted timing pulses (Fig. 9b, label wide bw received clock).
- A counter or random walk counter (Fig. 9b, label 956) for counting the early signals and lag signals (Fig. 9b, label 952), wherein multiple

frames of data is received (Col. 2, lines 61-67 and Col. 3, lines 1-5), the count would be performed for a plurality of bit periods.

- A threshold comparator (Fig. 9b, label 966) for comparing the count outputted by the counter (Fig. 9b, label 956) with a predetermined threshold (Fig. 9b, label 964) and
- A timing pulse delay adjustor (Fig. 9b, labels 970,974,976 and Fig. 4, label 436) for adjusting the timing pulse delay communicated to the phase detector (Fig. 9b, label 950) for adjusting the phase of the adjusted timing pulses (Col. 4, lines 18-39), which inherently adjusts the time or delays the pulses. The adjustment to the timing pulses occurs when the count exceeds the predetermined threshold. (Col. 9, lines 15-30) The phase detector synchronizes the delayed or adjusted timing pulses with the data transition pulses (Fig. 9b, label 950), wherein the data transition pulses are generated from the received signals. The received signals contain bits within a frame and multiple frames are received. (Col. 2, lines 51-67 and Col. 3, lines 1-5)

b. **Claim 2**, Marko et al discloses a data detector (Fig. 9b, label 948), wherein the transition detector detects and generates transitions by sampling the received signal. (Col. 8, lines 62-67)

c. **Claim 3**, Marko et al discloses "the predetermined wide loop BW value 964 set by the controller 962 is preferably less than 20…", which indicates the controller sets the value of the predetermined threshold or predetermined wide loop BW

value on some value that is preferably less than 20. Such a value can be selected to be any value as long as the above criterion is maintained. (Col. 9, lines 24-29)

d. **Claim 5,**

i. Marko et al teaches

- "a count magnitude generator for generating the magnitude count from the running count," (see the output magnitude from the early/late count Fig. 9, label 960)
- "the magnitude count being fed to the threshold count comparator for determining when the running count exceeds the predetermined first threshold count value, and" (see input to a comparator, which compares the count with a threshold (Fig. 9, label 966)
- "a count sign clipper for generating a count sign from the running count, the count sign being fed to the timing pulse delay adjustor for generating a timing pulse delay to adjust the adjusted timing pulses," (see sign outputted from label 956 in Fig. 9b)
- "the sign count for increasing the timing pulse delay when the data transition pulses arrive late relative to the adjusted timing pulses and for decreasing the timing pulse delay when the data transition pulses arrive early relative to the adjusted timing pulses" (see Col. 3, lines 55-66 which explains counts up for a lead and down for lag)

e. **Claim 6**,

i. Marko et al discloses

- "a data transition pulse generator for generating the data transition pulses" (see Fig. 9b, label 948)
- " a timing delay for delaying reference timing pulses into the adjusted timing pulse" (see Fig. 9b, labels 970,975,978)
- "a lead and lag generator for generating lead and lag signals for early and late arrivals of the data transition pulses relative to the adjusted timing pulses" (see Fig. 9b, labels 952 and 950).

f. **Claim 7** recites similar limitations regarding the "data transition pulse generator …", "timing delay …", "data transition pulse counter …", and "lead and lag generator …" as claim 6. The rejection for claim 7 regarding the limitations stated above is as stated for claim 6.

i. Claim 6 does not recite the limitation "when one and only one data transition pulse occurs within each search window following an adjusted timing pulse".

ii. Marko et al discloses receiving input bits within a frame, wherein the received signal is used within the transition detector and the phase detector (Fig. 9b, labels 948,950 and Col. 2, lines 51-67 and Col. 3, lines 1-5). Thus, the phase detector would detect a lead or lag between the data transition pulses (Fig. 9b, output from label 948) and the adjusted timing pulses (Fig. 9b, labels 970,974,980 and Fig. 4, label 436) would be detected within the frame of the received signal.

g. **Claim 9**, Regarding the limitation "the random walk counter sums the lead signals and lag signals as the running count", Marko et al discloses an early/late accumulator for summing the number of lead and lags. (Fig. 9b, label 956)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 4,8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Marko et al (US Patent No.: 5463351) in view of Carlson (US Patent No.: 6167526).

   a. **Claim 4,**

      i. Marko et al teaches "a threshold count value selector for selecting the first threshold count value" by disclosing a controller for selecting a value less than 20 to be used by the comparator (Fig. 9b, label 962,966 and Col. 9, lines 24-29 and please refer to the rejection of claim 3 for further explanation of the threshold selector)

      ii. Marko et al fails to discloses "an adaptive means for monitoring the rate at which the timing pulse delay is adjusted, the threshold value count selector adaptively selecting different first threshold count values when the

adjustment rate exceeds a predetermined rate being a second threshold count value".

- Carlson discloses a timing system updating or selecting the parameters of a window based on the predetermined value is less than the count of the early/late pulses. (Col. 3, lines 45-52) and an adaptive means, which updates or selects a new threshold when the predetermined rate is less than the adjustment rate or the second threshold count value. (Col. 3, lines 45-52, Fig. 4, Fig. 3, labels 380,390,x0-x3)
- Thus, it would be obvious to one skilled in the art to incorporate Carlson's invention into Marko et al's invention to provide more robust detection circuit, which is "less susceptible and sensitive to noise error."

b. **Claim 8** recites similar limitations regarding the "data transition pulse generator …", "timing delay …", "data transition pulse counter …", and "lead and lag generator …" as claim 7. The rejection for claim 8 regarding the limitations stated above is as stated for claim 7.

i. Claim 7 does not recite the limitation "a window delay for delaying the data transition pulses by half of a search window to center the data transition pulses within respective search windows".

ii. Carlson discloses a window detection unit (Fig. 3, label 308), wherein the windows of the early and late detectors (Fig. 3, labels 320 and 322) is controlled by unit label 308. Thus, when one data transition pulse is detected to be either early or late within the window, the counter is

increased or decreased (Fig. 3, label 370) and the adjusted timing pulses are produced. (Fig. 3, labels 308 and Col. 4, lines 26-32)

3. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable by Marko et al (US Patent No.: 5463351) in view of Ishizu (US Patent No.: 5661765).

a. **Claim 10**,

i. Marko et al disclose

- A data transition generator (Fig. 9b, label 948) for generating data transition pulses from a received baseband signal (Col. 7, lines 30-33, Col. 1, lines 55-62), wherein the received signal is inherently a self clocked signal. The received signals are further transmitted/received by a receiver front end coupled to a time division multiplexor for providing time division multiplexed framed digital signals. Framed digital signals would inherently comprise multiple or many bits within a frame or period. (Col. 2, lines 51-67 and Col. 3, lines 1-5) Since the data transition pulses are generated from the received signals, wherein the received signals contain bits within a frame, the data transition pulses are in synchronous with the received signal.
- A phase detector (Fig. 9b, label 950) for comparing the data transition pulses (Fig. 9b, label 948) with the adjusted timing pulses (Fig. 9b, label wide BW recovered clock) for generating early and late signals (Fig. 9b, labels early/late), wherein the early and late signals are inherently

generated when the data transition pulses (Fig. 9b, output from label 948) leads or lags the adjusted timing pulses (Fig. 9b, label wide bw received clock).

- A counter or random walk counter (Fig. 9b, label 956) for counting the early signals and lag signals (Fig. 9b, label 952), wherein multiple frames of data is received (Col. 2, lines 61-67 and Col. 3, lines 1-5), the count would be performed for a plurality of bit periods.
- A threshold comparator (Fig. 9b, label 966) for comparing the count outputted by the counter (Fig. 9b, label 956) with a predetermined threshold (Fig. 9b, label 964) and
- A timing pulse delay adjustor (Fig. 9b, labels 970,974,976 and Fig. 4, label 436) for adjusting the timing pulse delay communicated to the phase detector (Fig. 9b, label 950) for adjusting the phase of the adjusted timing pulses (Col. 4, lines 18-39), which inherently adjusts the time or delays the pulses. The adjustment to the timing pulses occurs when the count exceeds the predetermined threshold. (Col. 9, lines 15-30) The phase detector synchronizes the delayed or adjusted timing pulses with the data transition pulses (Fig. 9b, label 950), wherein the data transition pulses are generated from the received signals. The received signals contain bits within a frame and multiple frames are received. (Col. 2, lines 51-67 and Col. 3, lines 1-5)

ii. Marko et al fails to disclose "a pulse detector for generating data transition pulses from the zero crossings of the baseband signal waveform".

iii. Ishizu discloses such a limitation. (Col. 3, lines 10-16 disclose the zero crossing information found within the signal is determined for significant/insignificant or lead/lag. Col. 2, lines 35-37 discloses "A sign bit (MSB: {1,0}) represented in the form of a baseband waveform, of the output of the demodulator 2 is inputted to the phase comparator 3." Fig. 18(a) shows a diagram of a sample of a baseband signal. Fig. 16, label 3 shows a phase comparator.) It would have been obvious to one skilled in the art to incorporate a pulse detector for generating data transition pulses from the zero crossings of the baseband signal waveform" as disclosed by Ishizu into Marko et al's invention so to maintain phase synchronization.

4. **Claim 11** is rejected under 35 U.S.C. 103(a) as being unpatentable by Marko et al in view of Ishizu as applied to claim 10, further in view of Downey et al (US Patent No.: 5553081).

a. **Claim 11**, Marko et al in view of Ishizu fails to disclose "the baseband waveform signal having zero crossings encodes the digital bit stream using a modulation method selected from the group consisting of BPSK, QPSK, GMSK, 16-QAM and 64-QAM". Downey et al discloses such a limitation. (Col. 18, lines 43-44, lines 45-46) It would have been obvious to one skilled in the art to modulate or demodulate as disclosed by Downey et al and incorporate such a scheme into

Marko et al in view of Ishizu's invention so to provide a demodulated/modulated signal based on such modulation scheme.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
   a. Surie et al (US Patent No.: 4599735)
   b. Fujii (US Patent No.: 5349309)
   c. Kuramatsu (US Patent No.: 5440298)
   d. Sakaue et al (US Patent No.: 5577080).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).
7. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LINDA WONG whose telephone number is (571)272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Linda Wong
4/9/2008

/David C. Payne/

Supervisory Patent Examiner, Art Unit 2611